In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph at page 5, lines 6 to 26 as follows:

--Table 4 shows the truth table for the 32-bit overflow detector function for shifters. This table can be applied directly to generation of the logic of Figures 2A and 2B which are most similar in organization to that of the conventional 16-Bit shifter overflow detector function of Figure 1. It is worthwhile to point out that in the design of many high speed logic functions optimal propagation delay performance dictates that each gate have a relatively small number of inputs. Often it is desirable to use cascaded two input ~~gats~~ gates in preference to less levels of gates ~~have~~ having a large number of inputs (e.g. 8-input gates). Also it is sometimes preferable to use cascaded NAND gates to implement the logical equivalent of and AND-OR function for example. The cascaded NAND function appears in several parts of the logic of Figures 2A and 2B. One example is noted with NAND gates 211, 212, and 213 cascaded with NAND gate 205. Notice that in both the conventional 16-bit overflow function of Figure 1 and the conventional 32-bit shifter of Figures 2A and 2B, decoding of the shift value precedes the input of data in the logic path. Levels 101, 102 perform the shift decoding in Figure 1. Levels 201 and 202 perform shift value decoding in Figures 2A and 2B.--